



SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320

Important Instructions to examiners:

- 1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
- 2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
- 3) The language errors such as grammatical, spelling errors should not be given more importance (Not applicable for subject English and Communication Skills).
- 4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
- 5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
- 6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
- 7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q. N.	Answers	Marking Scheme																																								
1	(A)	Attempt any FIVE of the following:	10- Total Marks																																								
	(a)	List the binary, octal and hexadecimal numbers for decimal no. 0 to 15	2M																																								
	Ans:	<table border="1"> <thead> <tr> <th>DECIMAL</th> <th>BINARY</th> <th>OCTAL</th> <th>HEXADECIMAL</th> </tr> </thead> <tbody> <tr><td>0</td><td>0000</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0001</td><td>1</td><td>1</td></tr> <tr><td>2</td><td>0010</td><td>2</td><td>2</td></tr> <tr><td>3</td><td>0011</td><td>3</td><td>3</td></tr> <tr><td>4</td><td>0100</td><td>4</td><td>4</td></tr> <tr><td>5</td><td>0101</td><td>5</td><td>5</td></tr> <tr><td>6</td><td>0110</td><td>6</td><td>6</td></tr> <tr><td>7</td><td>0111</td><td>7</td><td>7</td></tr> <tr><td>8</td><td>1000</td><td>10</td><td>8</td></tr> </tbody> </table>	DECIMAL	BINARY	OCTAL	HEXADECIMAL	0	0000	0	0	1	0001	1	1	2	0010	2	2	3	0011	3	3	4	0100	4	4	5	0101	5	5	6	0110	6	6	7	0111	7	7	8	1000	10	8	2M
DECIMAL	BINARY	OCTAL	HEXADECIMAL																																								
0	0000	0	0																																								
1	0001	1	1																																								
2	0010	2	2																																								
3	0011	3	3																																								
4	0100	4	4																																								
5	0101	5	5																																								
6	0110	6	6																																								
7	0111	7	7																																								
8	1000	10	8																																								



SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320

		9	1001	11	9														
		10	1010	12	A														
		11	1011	13	B														
		12	1100	14	C														
		13	1101	15	D														
		14	1110	16	E														
		15	1111	17	F														
(b)	Define fan-in and fan-out of a gate.						2M												
Ans:	<p>Fan-in is a term that defines the maximum number of digital inputs that a single logic gate can accept. Most transistor-transistor logic (TTL) gates have one or two inputs, although some have more than two. A typical logic gate has a fan-in of 1 or 2.</p> <p>Fan-out is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed. Most transistor-transistor logic (TTL) gates can feed up to 10 other digital gates.</p>						1M 1M												
(c)	Compare between synchronous and asynchronous counter (any two points).						2M												
Ans:	<table border="1"> <thead> <tr> <th>Synchronous Counter</th> <th>Asynchronous Counter</th> </tr> </thead> <tbody> <tr> <td>All flip flops are triggered with same clock.</td> <td>Different clock is applied to different flip flops.</td> </tr> <tr> <td>It is faster.</td> <td>It is lower</td> </tr> <tr> <td>Design is complex.</td> <td>I Design is relatively easy.</td> </tr> <tr> <td>Decoding errors not present.</td> <td>Decoding errors present.</td> </tr> <tr> <td>Any required sequence can be designed</td> <td>Only fixed sequence can be designed.</td> </tr> </tbody> </table>						Synchronous Counter	Asynchronous Counter	All flip flops are triggered with same clock.	Different clock is applied to different flip flops.	It is faster.	It is lower	Design is complex.	I Design is relatively easy.	Decoding errors not present.	Decoding errors present.	Any required sequence can be designed	Only fixed sequence can be designed.	Any two 1M for each compari son
Synchronous Counter	Asynchronous Counter																		
All flip flops are triggered with same clock.	Different clock is applied to different flip flops.																		
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SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320

(d)	State two specification of DAC.		2M
Ans:	<p>1.Resolution: Resolution is defined as the ratio of change in analog output voltage resulting from a change of 1 LSB at the digital input VFS is defined as the full scale analog output voltage i.e. the analog output voltage when all the digital input with all digits 1. $Resolution = VFS / (2^n - 1)$</p> <p>2. Accuracy: Accuracy indicates how close the analog output voltage is to its theoretical value. It indicates the deviation of actual output from the theoretical value. Accuracy depends on the accuracy of the resistors used in the ladder, and the precision of the reference voltage used. Accuracy is always specified in terms of percentage of the full scale output that means maximum output voltage</p> <p>3. Linearity: The relation between the digital input and analog output should be linear. However practically it is not so due to the error in the values of resistors used for the resistive networks.</p> <p>4. Temperature sensitivity: The analog output voltage of D to A converter should not change due to changes in temperature. But practically the output is a function of temperature. It is so because the resistance values and OPAMP parameters change with changes in temperature.</p> <p>5. Settling time: The time required to settle the analog output within the final value, after the change in digital input is called as settling time. The settling time should be as short as possible.</p> <p>6. Long term drift Long term drift are mainly due to resistor and semiconductor aging and can affect all the characteristics. Characteristics mainly affected are linearity, speed etc.</p> <p>7. Supply rejection Supply rejection indicates the ability of DAC to maintain scale, linearity and other important characteristics when the supply voltage is varied. Supply rejection is usually specified as percentage of full scale change at or near full scale voltage at 25°C</p> <p>8. Speed: It is defined as the time needed to perform a conversion from digital to analog. It is also defined as the number of conversions that can be performed per second.</p>		Any two, 1M for each

SUMMER-19 EXAMINATION

Subject Name: Digital technique

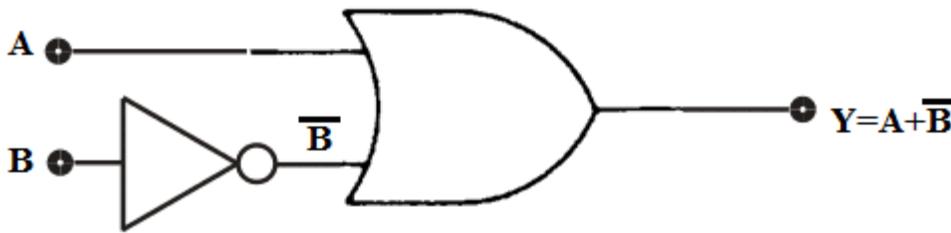
Model Answer

Subject Code:

22320

e)	Write the gray code to given no. $(1101)_2 = (?)$ Gray.	2M	
Ans:	<p>$(1101)_2 = (1011)$ Gray</p>	2M	
f)	Define encoder, write the IC number of IC used as decimal to BCD encoder.	2M	
Ans:	<p>An encoder is a device or circuit that converts information from one format or code to another, for the purpose of standardization, speed or compression.</p> <p>Decimal to BCD encoder IC- 74147</p>	<p>Defination-1M</p> <p>IC-1M</p>	
g)	Draw the logical symbol of EX-OR and EX-NOR gate.	2M	
Ans:	<p><u>EX-OR GATE:-</u></p> <p>$A \cdot \bar{B} + \bar{A} \cdot B$</p> <p><u>EX-NOR GATE:-</u></p> <p>$A \cdot B + \bar{A} \cdot \bar{B}$</p>	<p>EX-OR-1M</p> <p>EX-NOR-1M</p>	
Q. No.	Sub Q. N.	Answers	Marking Scheme
2		Attempt any THREE of the following:	12- Total Marks

$$\begin{aligned}
 Y &= A + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + ABC + \bar{A}\bar{B} \\
 &= A(1 + BC) + \bar{A}\bar{B}(C + \bar{C}) + \bar{A}\bar{B} \\
 &= A + \bar{A}\bar{B} + \bar{A}\bar{B} \\
 &= A + \bar{A}\bar{B} \\
 &= (A + \bar{A}) \cdot (A + \bar{B}) \\
 &= (A + \bar{B})
 \end{aligned}$$



c) Explain the following characteristics w.r.t. logic families :

- (i) Noise margin
- (ii) Power dissipation
- (iii) Figure of merit
- (iv) Speed of operation

4M

Ans: Noise margin indicates the amount to noise voltage circuit can tolerate at its input for both logic 1 and logic 0.

Power Dissipation: It is the amount of power dissipated in an IC.

Figure of Merit: It is defined as the product of propagation delay and power dissipated by

1M each
definition

SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320

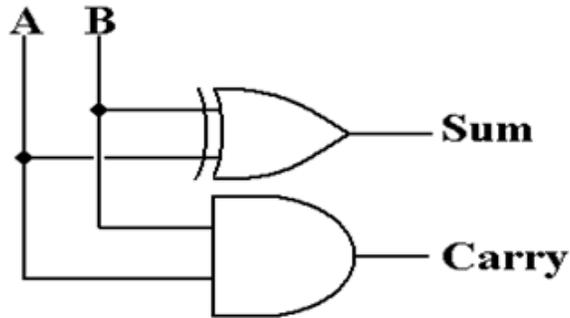
the gate.

Speed of Operation: Speed of a logic circuit is determined by the time between the application of input and change in the output of the circuit.

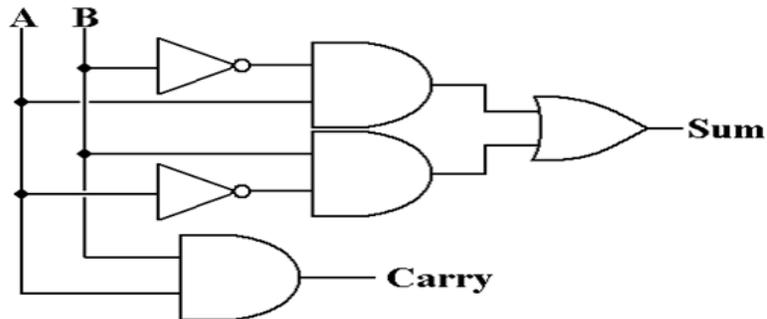
d) Draw logic diagram of half adder circuit

4M

Ans:



OR



Note: logic diagram using NAND/NOR also can be considered.

4M

Q. No.	Sub Q. N.	Answers	Marking Scheme
3		Attempt any THREE of the following :	12- Total Marks

SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320

a) Draw the circuit of successive approximation type ADC and explain its working

4M

Ans:

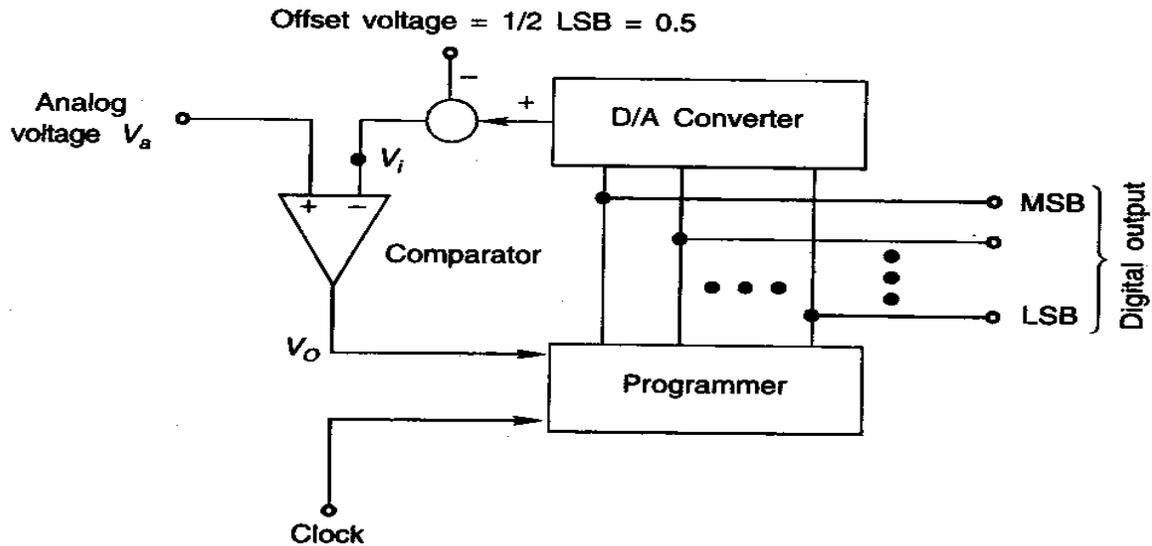


Diagram
2M

The successive approximation A/D converter is as shown in fig. An analog voltage (V_a) is constantly compared with voltage V_i , using a comparator. The output produced by comparator (V_o) is applied to an electronic Programmer.

If $V_a = V_i$, then $V_o = 0$ & then no conversion is required. The programmer displays the value of V_i in the form of digital O/P.

But if $V_a < V_i$, then the O/P is changed by the programmer.

If $V_a > V_i$, then value of V_i is increased by 50% of earlier value.

But if $V_a < V_i$, then value of V_i is decreased by 50% of earlier value.

This new value is converted into analog form, by D/A converter so as to compare it with V_a again. This procedure is repeated till we get $V_a = V_i$. As the value of V_i is changed successively, this method is called as successive-approximation A/D converter.

Explanat
ion 2M

b) Describe the operation of R-S flip flop using NAND gates only .

4M

Ans:

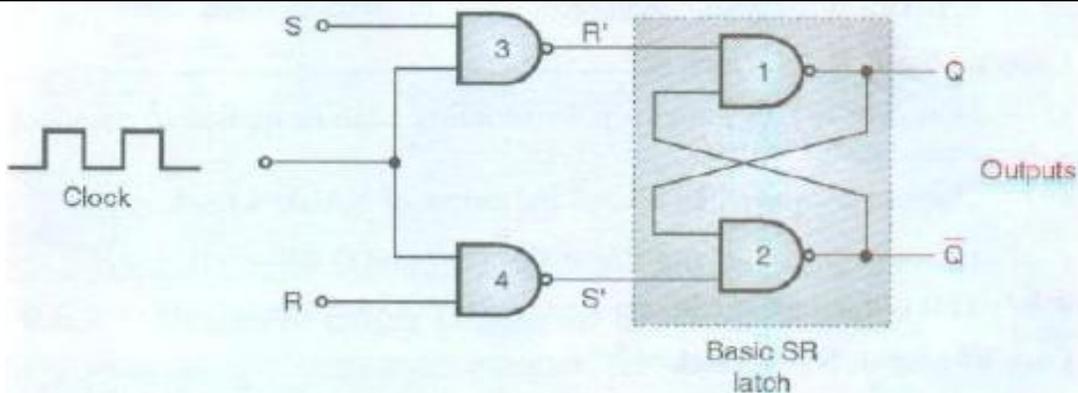
SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320



Description/explanation-

When clock = 0, the outputs of NAND gates 3 and 4 will be forced to be 1 irrespective of the values of S and R. That means $R' = S' = 1$. Hence the outputs of basic SR/F/F i.e. Q_{n+1} and \overline{Q}_{n+1} will not change. Thus if clock = 0, then there is no change in the output of the clocked SR flip-flop.

Case I : S = R = 0, clock = 1: No change

If $S=R=0$ then outputs of NAND gate 3 and 4 are forced to become 1. Hence R' and S' both will be equal to 1. Since R' and S' are the inputs of the basic S – R flip-flop using NAND gates. There will be no change in the state of outputs.

Case II : S =1, R = 0, clock = 1: Set

Now $S=0, R=1$ and a positive going edge is applied to the clock
Output of NAND 3 i.e. $R' = 0$ and output of NAND 4 i.e. $S' = 1$.
Hence output of SR flip-flop is $Q_{n+1} = 1$ and $\overline{Q}_{n+1} = 0$.
This is the set condition.

Case III : S =0, R = 1, clock = 1: Reset

Now $S=0, R=1$ and a positive edge is applied to the clock input.
Since $S=0$, output of NAND – 3 i.e. $R' = 1$. And as $R' = 1$ and clock = 1 the output of NAND-4 i.e. $S' = 0$. Hence output of SR flip-flop is $Q_{n+1} = 0$ and $\overline{Q}_{n+1} = 1$.
This is the reset condition.

Case IV : S =1, R = 1, clock = 1: Undefined/ forbidden

As $S=1, R=1$ and clock = 1, the outputs of NAND gates 3 and 4 both are 0 i.e. $S' = R'=0$. So both the outputs $Q_{n+1} = 1$ and $\overline{Q}_{n+1} = 1$
Hence output is Undefined/ forbidden.

Logical
Diagram
2M

Explanat
ion 2M

Explanat
ion
without
clock
pulse
must
also be
consider
ed



SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

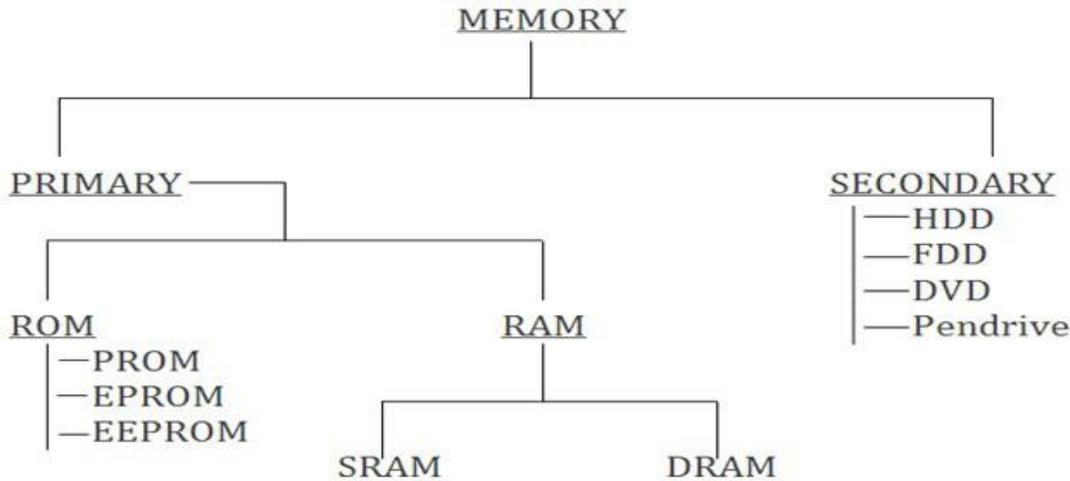
22320

CLK	INPUTS		OUTPUTS		REMARK
	S	R	Q_{n+1}	$\overline{Q_{n+1}}$	
0	X	X	Q_n	$\overline{Q_n}$	No change
1	0	0	Q_n	$\overline{Q_n}$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	?	?	Forbidden

c) Give classification of memory and compare RAM and ROM (any four points)

4M

Ans: classification of memory



Classification
2M
Consider even if
Secondary
memory
is not
written

Comparison between RAM and ROM

RAM	RAM
1. Temporary Storage.	1. Permanent Storage.
2. Store data in MBs.	2. Store data in GBs.
3. Volatile .	3. Non-Volatile



SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320

	4. Writing data is Faster.	4. Writing data is Slower.	Comparison 2M
d)	State the applications of shift register.		
Ans:	<p>1] Shift register is used as Parallel to serial converter, which converts the parallel data into serial data. It is utilized at the transmitter section after Analog to Digital Converter (ADC) block.</p> <p>2] Shift register is used as Serial to parallel converter, which converts the serial data into parallel data. It is utilized at the receiver section before Digital to Analog Converter (DAC) block.</p> <p>3] Shift register along with some additional gate(s) generate the sequence of zeros and ones. Hence, it is used as sequence generator.</p> <p>4] Shift registers are also used as counters. There are two types of counters based on the type of output from right most D flip-flop is connected to the serial input. Those are Ring counter and Johnson Ring counter.</p>		Each Application 1M Any other relevant application must be considered

Q. No.	Sub Q. N.	Answers	Marking Scheme
4		Attempt any THREE of the following :	12- Total Marks
	(a)	<p>Subtract the given number using 2's compliment method:</p> <p>(i) $(11011)_2 - (11100)_2$</p> <p>(ii) $(1010)_2 - (101)_2$</p>	4M
	Ans:	<p>i) Subtract $(11011)_2 - (11100)_2$ using 2's complement binary arithmetic.</p> <p>Solution:</p> <p>$(11011)_2 - (11100)_2$</p> <p>Now,</p> <p>2's complement of $(11100)_2 = 1$'s complement of $(11100)_2 + 1$</p> <p>1's complement of $(11100)_2 = (00011)_2$</p>	2's complement



SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320

2's complement = $00011+1 = 00100$

$$\begin{array}{r} \text{Therefore,} \qquad \qquad \qquad 1 \ 1 \ 0 \ 1 \ 1 \\ + \qquad \qquad \qquad \qquad \qquad 0 \ 0 \ 1 \ 0 \ 0 \\ \hline \qquad \qquad \qquad \qquad \qquad 1 \ 1 \ 1 \ 1 \ 1 \end{array}$$

There is no carry it indicates that results is negative and in 2's complement form i.e. $(11111)_2$.

Therefore, for getting true value i.e. $(+1)$ take 2's complement of (11111) is

1's complement + 1

= $00000 + 1$

Ans= $(00001)_2$

Ans: $(11011)_2 - (11100)_2 = 2's \text{ complement of } (11111)_2 = (-1)_{10}$

ii) **Subtract $(1010)_2 - (101)_2$ using 2's complement binary arithmetic.**

2's complement of $(0101)_2 = 1's \text{ complement of } (0101)_2 + 1$

1's complement of $(0101)_2 = (1010)_2$

2's complement = $1010+1 = 1011$

$$\begin{array}{r} \text{Therefore,} \qquad \qquad \qquad 1 \ 0 \ 1 \ 0 \\ + \qquad \qquad \qquad \qquad \qquad 1 \ 0 \ 1 \ 1 \\ \hline \qquad \qquad \qquad \qquad \qquad 1 \\ \qquad \qquad \qquad \qquad \qquad 1 \ 0 \ 1 \ 0 \ 1 \end{array}$$

There is carry ignore it, which indicates that results is positive i.e. $(+5)$

= $(0101)_2$

Ans: $(1010)_2 - (101)_2 = (0101)_2 = (+5)_{10}$

1M

Final
Answer-
1M

2's
comple
ment
1M

Final
Answer-
1M

(b) **Stare De-Morgan's theorem and prove any one**

4M



SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320

Ans:

De Morgan's 1st Theorem:

It states that the compliment of sum is equal to the product of the compliment of individual variables.

$$\overline{(A + B)} = \bar{A} \bar{B}$$

Proof:

A	B	\bar{A}	\bar{B}	A+B	$\overline{(A+B)}$	$\bar{A} \bar{B}$
0	0	1	1	0	1	1
0	1	1	0	1	0	0
1	0	0	1	1	0	0
1	1	0	0	1	0	0

De Morgan's 2nd Theorem:

It states that the compliment of product is equal to the sum of the compliments of individual variables.

$$\overline{(A B)} = \bar{A} + \bar{B}$$

Proof:

A	B	\bar{A}	\bar{B}	A.B	$\overline{(A B)}$	$\bar{A} + \bar{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

Statements-1M each

Anyone proof - 2M

(c)

Compare between PLA and PAL.

4M



SUMMER-19 EXAMINATION

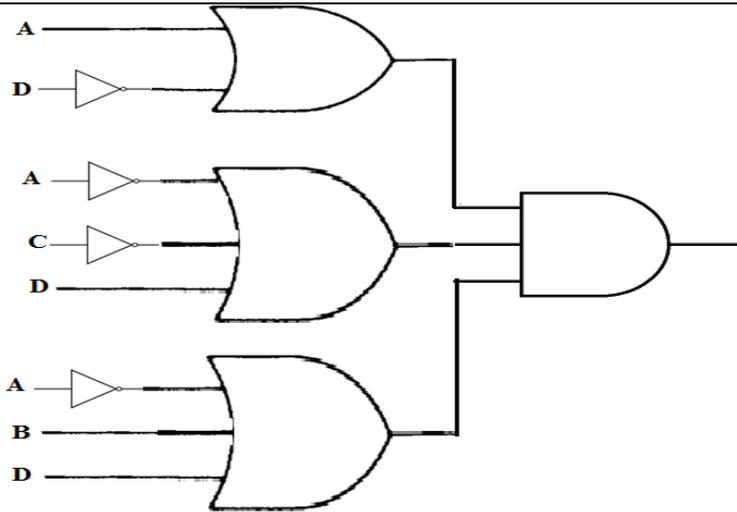
Subject Name: Digital technique

Model Answer

Subject Code:

22320

Ans:	<p style="text-align: center;">PLA</p> <ol style="list-style-type: none"> 1) Both AND and OR arrays are programmable 2) Costliest and complex than PAL 3) AND array can be programmed to get desired minterms. 4) Large number of functions can be implemented. 5) Provides more programming flexibility. 	<p style="text-align: center;">PAL</p> <ol style="list-style-type: none"> 1) OR array is fixed and AND array is programmable. 2) Cheaper and simpler 3) AND array can be programmed to get desired minterm. 4) Provides the limited number of functions. 5) Offers less flexibility, but more likely used. 	Any four 4 points- 1M each
(d)	<p>Reduce the following expression using K-map and implement it</p> <p>$F(A,B,C,D) = \sum m(1,3,5,7,8,10,14)$</p>		4M
Ans:	<p style="text-align: center;">$F(A,B,C,D) = (A + \bar{D}) (\bar{A} + \bar{C} + D) (\bar{A} + B + D)$</p>		Kmap- 1M Pairs- 1.5M Final Ans- 1.5M



(e) Describe the working of J-K flip-flop and state the race around condition.

4M

Ans:

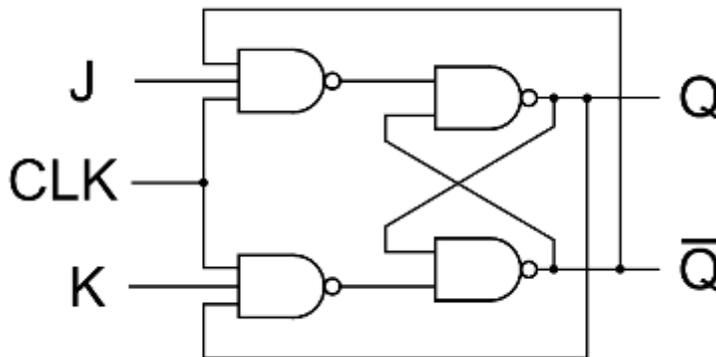


Diagram
-1.5M
Working
-1.5M
State-
1M

Inputs			Outputs		Comments
J	K	CLK	Q	\bar{Q}	
0	0	↑	Q_0	\bar{Q}_0	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	\bar{Q}_0	Q_0	Toggle

The clock signal is applied to CLK input.

IF CLK =0 than F/F is disabled and O/P Q and \bar{Q} do not change

SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320

If CLK= 1 and J=K=0 then the output Q and \bar{Q} will not change their state.

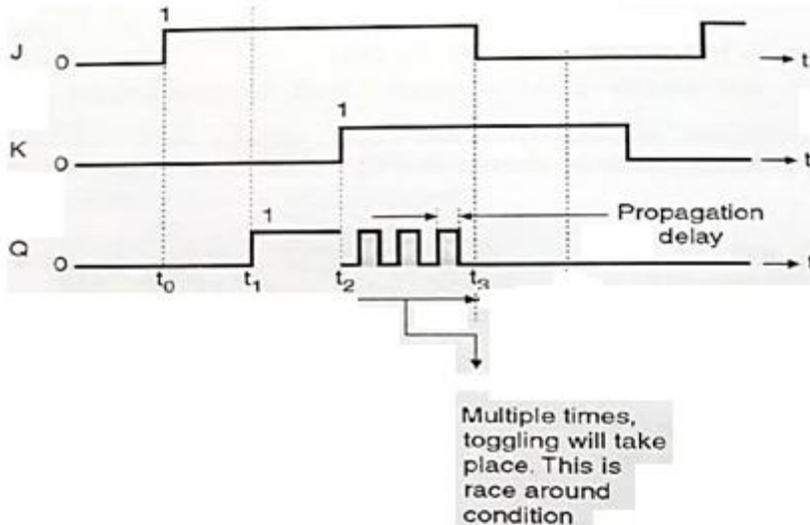
If J=0 and K= 1 then JK flip flop will reset and Q= 0 & \bar{Q} =1

If J=1 and K=0 then output will be set and Q=1 & \bar{Q} =0

If J= K=1 then Q & \bar{Q} outputs are inverted and FF will toggle

Race Around condition:

Race around condition occurs in J K Flip-flop only when J=K=1 and clock/enable is high (logic 1) as shown below-



In JK Flip-flop when J=K=1 and when clock goes high, output should toggle (change to opposite state), but due to multiple feedback, output changes/toggles many times till the clock/enable is high.

Thus toggling takes place more than once, called as racing or race around condition.

Q. No.	Sub Q. N.	Answers	Marking Scheme
5.		Attempt any TWO of the following:	12- Total Marks
	a)	Design BCD to seven segment decoder using IC 7447 with its truth table.	6M

SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

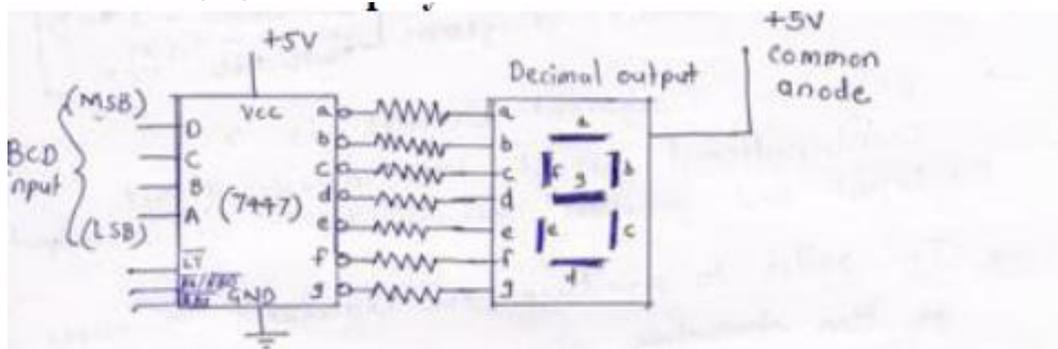
Subject Code:

22320

Ans: **Note: Any one type of display shall be considered**

1. BCD to 7 segment decoder is a combinational circuit that accepts 4 bit BCD input and generates appropriate 7 segment output.
2. In order to produce the required numbers from 0 to 9 on the display the correct combination of LED segments need to be illuminated.
3. A standard 7 segment LED display generally has 8 input connections, one from each LED segment & one that acts as a common terminal or connection for all the internal segments
4. Therefore there are 2 types of display 1. Common Anode Display 2. Common Cathode Display :

Common Anode Display



For normal functioning \overline{LT} , $\overline{BI}/\overline{RBO}$ & \overline{RBI} should be connected to logic 1

Truth Table

for seven segment decoder using common anode display

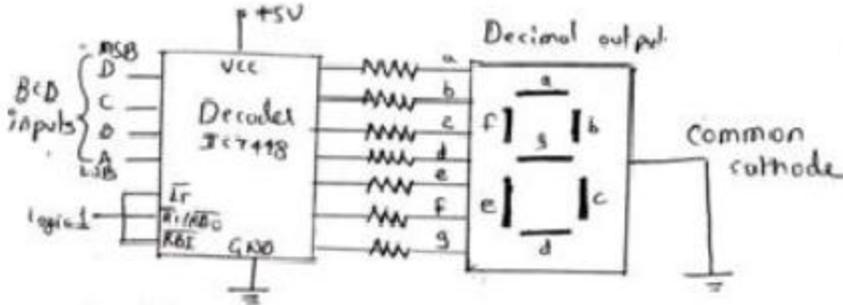
BCD Input				7 segment coded outputs							Display outputs
D	C	B	A	\overline{a}	\overline{b}	\overline{c}	\overline{d}	\overline{e}	\overline{f}	\overline{g}	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	0
0	0	1	0	0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0	1	1	0	0
0	1	0	0	1	0	0	1	1	0	0	0
0	1	0	1	0	1	0	0	1	0	0	0
0	1	1	0	1	1	0	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1	0
1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	1	0	0	0

Explanation 2M

Circuit Diagram 2M

Truth Table 2M

Common Cathode Display:



Truth Table

BCD inputs				→ segment coded outputs							Display output
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	1
0	0	1	1	1	1	1	1	0	0	1	1
0	1	0	0	0	1	1	0	0	1	1	1
0	1	0	1	1	0	1	1	0	1	1	1
0	1	1	0	0	0	1	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0	1
1	0	0	0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	0	1	1	1

b) Describe the working of 4 bit universal shift register.

6M

Ans:

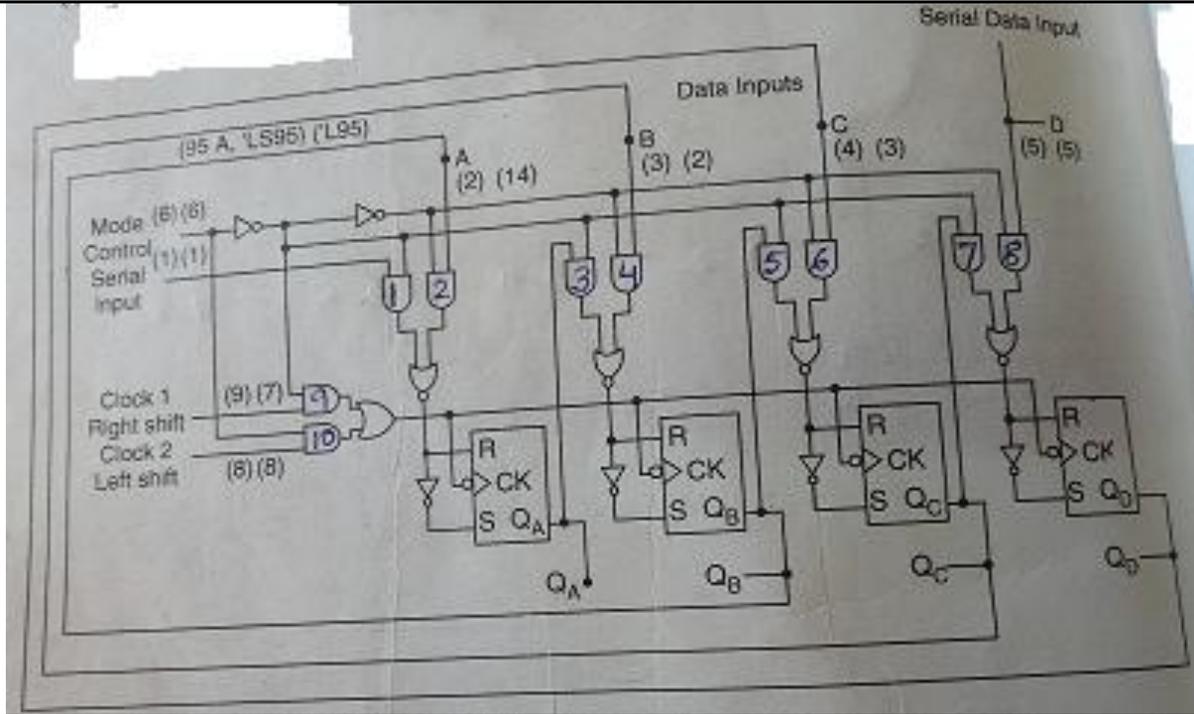
SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320



Circuit
Diagram
3M

Working
3M

Fig:4 bit universal shift register

Working:

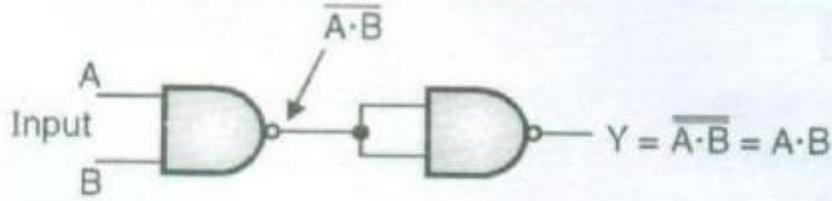
- 1. PARALLEL LOAD:** When mode control (M) is connected to logic 1, AND gates 2, 4, 6, 8 will be enabled and AND gates 1, 3, 5, 7, will be disabled. The 4-bit binary data will be loaded parallel. The clock-2 input will be applied to the flip-flops, since M= 1, AND gates -10 is enabled and gate-9 is disabled. Input will transfer parallel data to QA to QD outputs.
- 2. SHIFT RIGHT:** When mode control (M) is connected to logic 0, AND gates 1, 3, 5, 7 will be enabled and gates 2, 4, 6, 8, will be disabled. The data will be shifted serially. The clock -1, input will be applied to the flip-flops, Since M = 0, AND gates - 9 is enabled, and gates -10 is disabled. The data is shifted serially to right from QA to QD.
- 3. SHIFT LEFT:** When mode control (M) is connected to logic 1, AND gates 2, 4, 6, 8 will be enabled. This mode permits parallel loading of the register and shift-left operation. The shift-left operation can be accomplished by connecting the output of each flip flop to the parallel input of the previous flip-flop and serial input is applied at the input.

c) Design basic logic gates using NAND and NOR gate.

6M

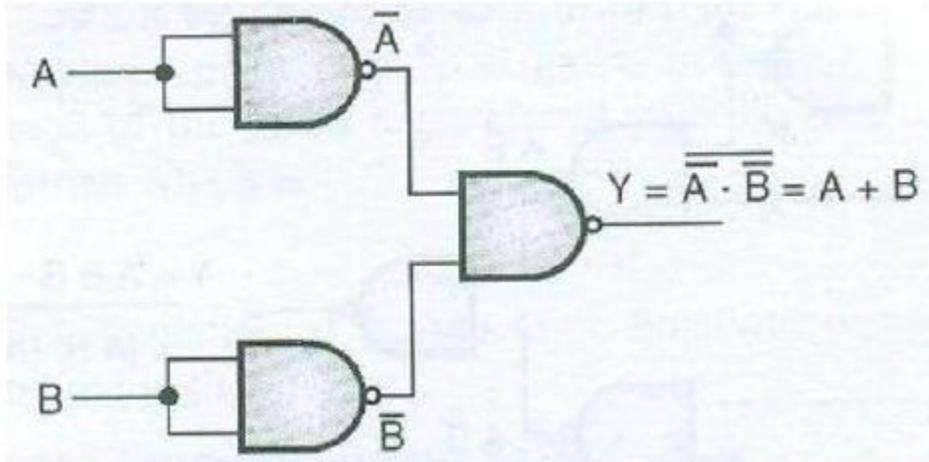
Ans:

AND gate using NAND

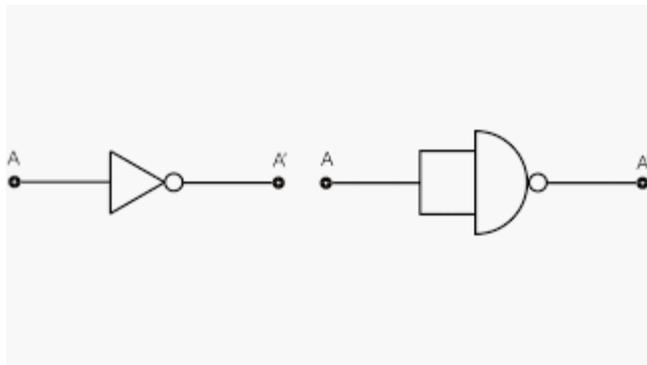


AND gate using NAND

OR gate using NAND



NOT gate using NAND $\overline{A \cdot A} = \overline{A}$



OR gate using NOR gate:

Expression for OR gate is $Y = \overline{\overline{A + B}} = A + B$

Each
Gate
Design
1 Marks

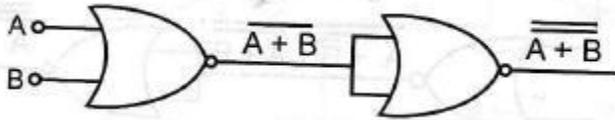
SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

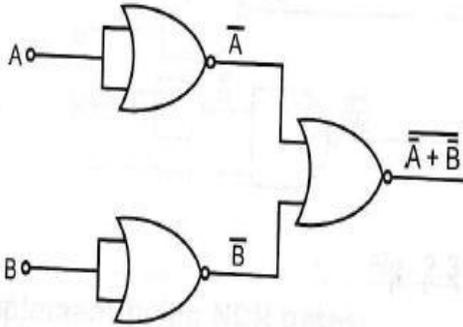
Subject Code:

22320

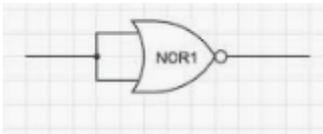


AND gate using NOR gate:

Expression for AND gate is $Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$ (Applying De Morgan's theorem)



NOT gate using NOR $Y = \overline{A + A} = \overline{A}$



Q. No.	Sub Q. N.	Answers	Marking Scheme
6.		Attempt any TWO of the following :	12- Total Marks
	a)	Design a mod-6 Asynchronous counter with truth-table and logic.	6M
	Ans:	MOD 6 asynchronous counter will require 3 flip flops and will count from 000 to 101. Rest of the states are invalid. To design the combinational circuit of valid states, following truth table and K-map is drawn:	Truth Table 2M

SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320

Q _C	Q _B	Q _A	Reset Logic
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

From the above truth table, we draw the K-maps and get the expression for the MOD 6 asynchronous counter.

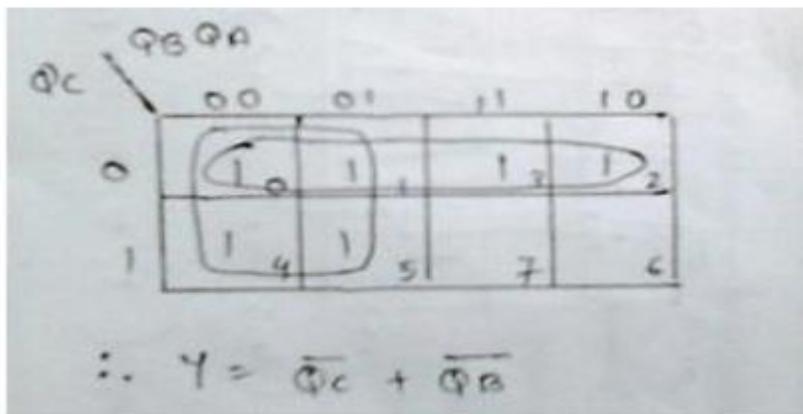


Fig: K-map for above truth table

Thus reset logic is OR of complemented forms of QC and QB. This will be given to the reset inputs of the counter so that as soon as count 110 reaches, the counter will reset. Thus the counter will count from 000 to 101. The implementation of the designed MOD 6 asynchronous counter is shown below:

Logic
Diagram
2M

Circuit
Diagram
2M

SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320

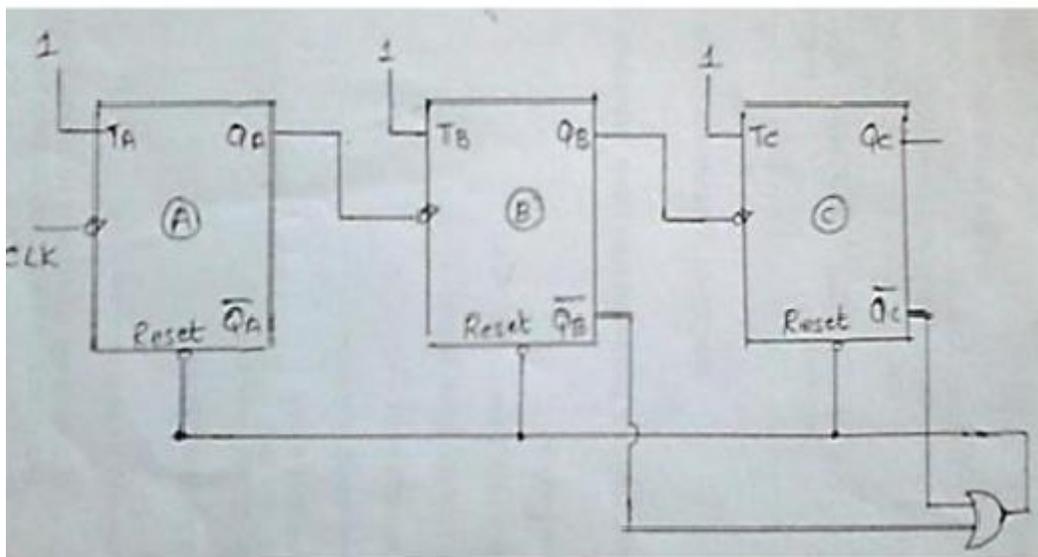


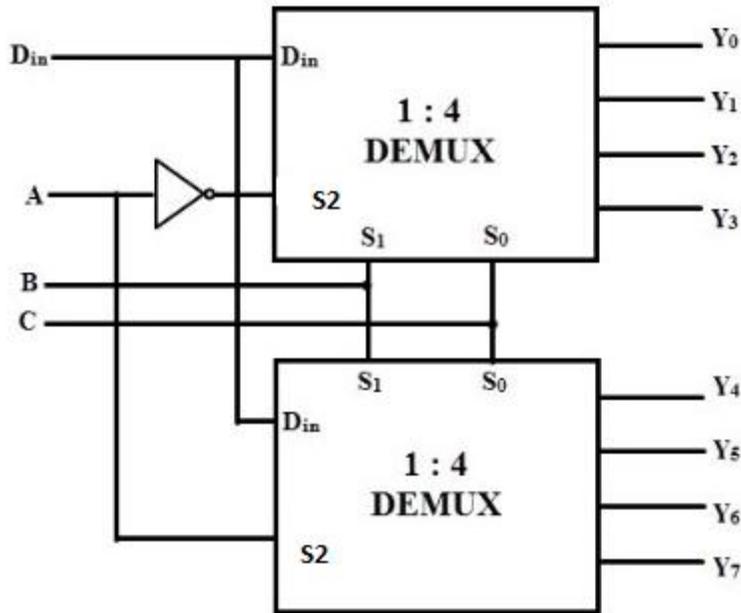
Fig: Circuit diagram of MOD 6 asynchronous counter

b) Design 1:8 de multiplexer using 1:4 de multiplexer

6M

Ans:

Design
3M



Truth
Table
3M

Fig:1:8 Demultiplexer using 1:4 demultiplexer

Data Input	Select Inputs			Outputs							
	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

Fig: Truth Table of 1:8 Demultiplexer .

c) Draw the circuit diagram of 4 bit R-2R ladder DAC and obtain its output voltage expression

6M

Ans:

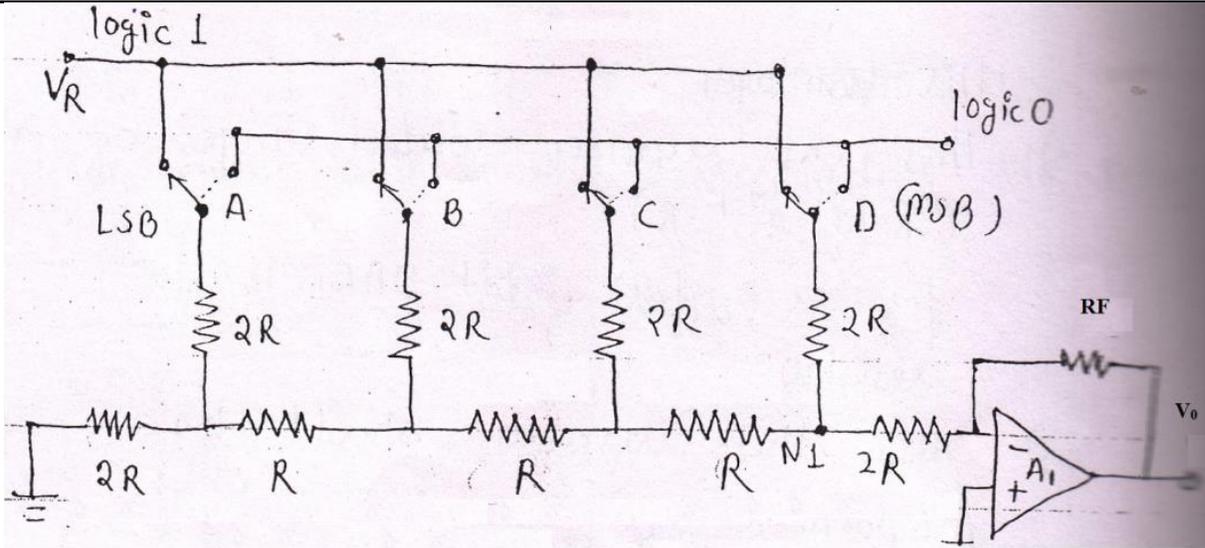
SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

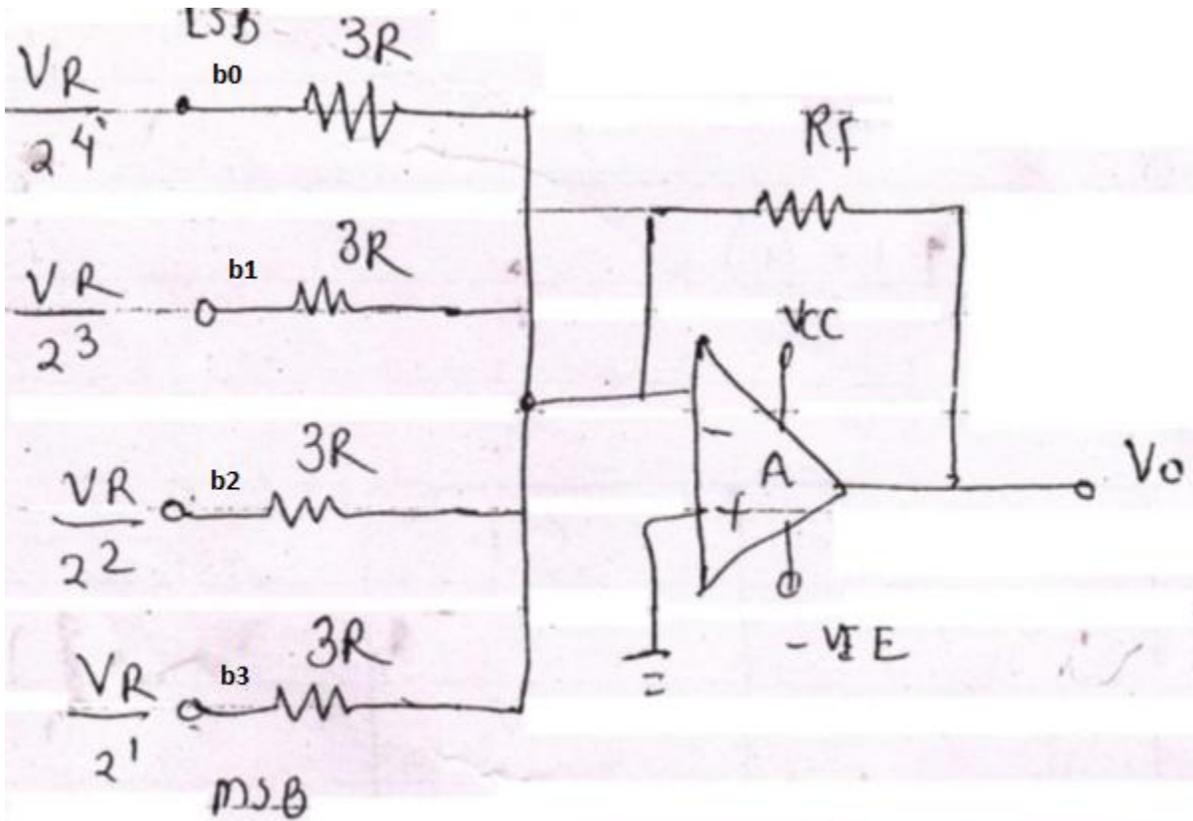
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22320



2M

Fig 1: 4 bit R-2R ladder DAC



2M

Fig 2: Simplified circuit diagram of Fig 1

Therefore output analog voltage V_o is given by,



SUMMER-19 EXAMINATION

Subject Name: Digital technique

Model Answer

Subject Code:

22320

$$V_o = - \left(\frac{R_f}{3R} \cdot \frac{V_R}{2^4} b_0 + \frac{R_f}{3R} \cdot \frac{V_R}{2^3} b_1 + \frac{R_f}{3R} \cdot \frac{V_R}{2^2} b_2 + \frac{R_f}{3R} \cdot \frac{V_R}{2^1} b_3 \right)$$

$$V_o = - \left(\frac{R_f}{3R} \right) \left(\frac{V_R}{2^4} \right) [8b_3 + 4b_2 + 2b_1 + b_0]$$

2M